REAL-TIME systems are systems that must respond to external stimuli in a timely fashion. The correctness of a real-time system depends on not only the logical correctness of its tasks but also the timeliness of their executions. The wide adoption of real-time technologies has already resulted in significant impacts on how automated systems are designed and deployed. They are key technologies needed to provide distributed and collaborative industrial environments. Solutions with better intelligence and flexibility are provided at lower cost and more functionality. In this Special Section, six papers are published with excellent results related to task scheduling, real-time control, and critical issues in development tool designs.

The first paper, entitled “Optimization-Based Dynamic Reconfiguration of Real-Time Schedulers With Support for Stochastic Processor Consumption,” proposes scheduling mechanisms to maximize the overall system benefit subject to schedulability constraints. Application modes are characterized by their required processing bandwidth and benefit values. Task execution times are described as probability distributions. Making use of this stochastic modeling one is able to dynamically reconfigure the scheduler subject to probabilistic schedulability guarantees.

The second paper, entitled “Parameter Selection for Real-Time Controllers in Resource-Constrained Systems,” presents a general methodology that integrates control issues and real-time schedulability analysis to improve the control performance in embedded systems with time and resource constraints. The performance increase is achieved by properly selecting task periods and deadlines under feasibility constraints.

The third paper, entitled “Optimizing the Software Architecture for Extensibility in Hard Real-Time Distributed Systems,” considers a set of control tasks that must be executed on distributed platforms so that end-to-end latencies are within deadlines. Authors investigate how to allocate tasks to nodes, pack signals to messages, allocate messages to buses, and assign priorities to tasks and messages, so that the design is extensible and robust with respect to changes in task requirements.

The fourth paper, entitled “Synthesis of Multitask Implementations of Simulink Models With Minimum Delays,” presents an improvement of code generation technology for Synchronous Reactive obtained via a novel algorithm for optimizing the multitask implementation of Simulink models on single-processor platforms with limited availability of memory. The proposed algorithm leverages a novel efficient encoding of the scheduling feasibility region to find the task implementation of function blocks with minimum additional functional delays within timing and memory constraints. The algorithm is applied to an automotive case study with tens of function blocks and very high utilization to test its applicability to complex systems.

The fifth paper, entitled “Time-Aware Instrumentation of Real-Time Programs,” proposes an instrumentation technique for debugging applications with temporal constraints with the purpose of enabling the developer to locate the origins of software misbehaviors. The proposed framework permits reasoning about space and time, and allows composition of software instrumentations. In particular, it introduces a low perturbation by optimizing the number of insertion points and trace buffer size for code size and time budgets. The theory is applied to two concrete case studies: the OpenEC firmware for the keyboard controller of the One Laptop Per Child project and the flash file system.

The sixth paper, entitled “Address-Independent Estimation of the Worst-Case Memory Performance,” presents an analytical model that provides fast, safe, and tight estimations of the worst-case cache performance, which plays a key role in the calculation of the upper bound of worst-case execution times. The main novelty of the proposed approach is that it requires no information about the base addresses of the data structures. This property is very interesting, since base addresses are sometimes unavailable at compile time, and they can change between different executions. The approach is also validated through extensive simulations.

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